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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,029	09/12/2003	Jyh Chain Lin		9296
25859	7590	05/17/2007	EXAMINER	
WEI TE CHUNG			ALMO, KHAREEM E	
FOXCONN INTERNATIONAL, INC.			ART UNIT	PAPER NUMBER
1650 MEMOREX DRIVE			2816	
SANTA CLARA, CA 95050				
MAIL DATE		DELIVERY MODE		
05/17/2007		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/662,029	LIN, JYH CHAIN	
	<b>Examiner</b>	<b>Art Unit</b>	
	Khareem E. Almo	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 27 February 2007.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-8 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-8 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 12 September 2003 is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application |
|  | 6) <input type="checkbox"/> Other: _____                          |

**DETAILED ACTION**

1. The amendments filed 2/27/2007 have been received and entered in the case.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 7 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by AAPA.

With respect to claim 1, figure 4 of Applicant's admitted Prior Art discloses a pulse width modulation current adjustment apparatus comprising: a triangle wave generator (1) for generating a triangle wave voltage signal; a modulation voltage source configured for providing a modulation voltage signal (6) a comparator (2), a field effect transistor (3), a power supply (7), a first resistor (4), and a second resistor (5); wherein the triangle wave voltage signal has a plurality of rising portions and a plurality of declining portions, the triangle wave voltage signal only comprises odd harmonics such that a percentage of high frequency harmonics of the triangle wave voltage signal is low; the triangle wave signal and the modulation signal are input to the comparator, and an output of the comparator is connected to a gate terminal of the field effect

Art Unit: 2816

transistor,, the first resistor is connected between the power supply (7) and a source terminals (S) of the field effect transistor, and a drain terminal (D) of the field effect transistor, outputs a pulse width modulation current signal driving current through the second resistor (5) to a load.

With respect to claim 2, figures 4 and 5 of AAPA disclose a pulse width modulation current adjustment apparatus as described in claim 1, wherein the triangle wave signal is a symmetric triangle wave signal (i.e. the individual triangles within each period form a perfect isosceles triangle with the base being the leftmost rising edge and the sides being the period and the right edge.)

With respect to claim 7, figure 4 of AAPA discloses a circuit in which the recited method of making a pulse width modulation current adjustment apparatus comprising the steps of: providing a triangle wave generator for generating a triangle wave signal, connecting a comparator to said triangle wave generator, connecting a voltage source to said comparator; connecting said comparator to a gate terminal of a field effect transistor; connecting a power supply to a source terminal via a first resistor and connecting a load to a drain terminal of the FET via a second resistor is inherent.

With respect to claim 8, figure 6 of AAPA, discloses a triangle wave generator used in a pulse width modulation current adjustment apparatus comprising a first operational amplifier (2); a front resistor (connected to ground) electrically connecting a negative terminal of the first operational amplifier (between R1 and D1) and ground; a first feedback resistor (R4) a second feedback resistor (R2) and a first current limiting resistor ((connected to positive terminal of first operational amplifier) so as to form a

Art Unit: 2816

zero-crossing comparator, a second operational amplifier (connected to  $u_0$ ) a second current limiting resistor ( $R_3$ ) and a capacitor ( $C$ ) together forming an integrator; a back grounding resistor ( $R_1$  grounded through  $U_z$ ) electrically connected to a positive terminal of the second operational amplifier (between  $R_1$  and  $D_1$ ) to ground; and an output of the first operational amplifier (between  $R_1$  and  $D_1$ ) electrically connected to said positive terminal of the first operational amplifier via said first current limiting resistor ( $R_4$ ) and an output of the second operational amplifier (connected to  $u_0$ ) electrically connected to the negative terminal of the second operational amplifier via the capacitor and also electrically connected to the positive terminal of the first operational amplifier via the second feedback transistor ( $R_2$ ), the output of the second operation amplifier outputting a triangle wave voltage signal, the triangle wave voltage signal having a plurality of rising portions and a plurality of declining portions, and the triangle wave voltage signal only comprising odd harmonics such that a percentage of high frequency harmonics of the triangle wave voltage signal is low.

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Figure 4 of AAPA.

With respect to claims 3-6, figure 4 discloses a pulse width modulation current adjustment apparatus as described in claim 1, wherein the field effect transistor is an N-channel type FET. It would be obvious to one skilled in the art at the time the invention was made to interchange different types of FET transistors for the purpose of optimizing the circuit to work in different environments. (i.e. to switch on a high signal, low signal etc.)

3. Claims 1 and 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haas (US 3621282).

With respect to claims 1, and 3-6, figure 4 of (US 3621282) discloses a pulse width modulation current adjustment apparatus comprising: a triangle wave generator for generating a triangle wave voltage signal (SAWTOOTH OUTPUT); a modulation voltage source (-6V) configured for providing a modulation voltage signal; a comparator (COMPARATOR), a transistor (Q1), a power supply (+12V or -6V), a first resistor (R4), and a second resistor (between Q1 and Q2); wherein the triangle wave voltage signal has a plurality of rising portions and a plurality of declining portions, the triangle wave voltage signal only comprises odd harmonics such that a percentage of high frequency harmonics of the triangle wave voltage signal is low; the triangle wave signal and the modulation signal are input to the comparator, and an output of the comparator is connected to a gate terminal of the transistor, the first resistor is connected between the power supply (+12V) and a terminal of the transistor, and a terminal of the transistor

Art Unit: 2816

outputs a pulse width modulation current signal through the second resistor to a load, but fails to disclose wherein the transistor is a FET. It would be obvious at the time the invention was made to a person having ordinary skill in the art to use any FET in place of the BJT for the purpose of more stable switching.

With respect to claim 7, the circuit above produces a circuit in which the recited method of making a pulse width modulation current adjustment apparatus comprising the steps of: providing a triangle wave generator for generating a triangle wave voltage signal, the triangle wave voltage signal having a plurality of rising portions and a plurality of declining portions, and the triangle wave voltage signal only comprising odd harmonics such that a percentage of high frequency harmonics of the triangle wave signal is low; comparing the triangle wave voltage signal with a modulation voltage signal supplied by a modulation voltage signal through a comparator to generate a digital pulse voltage signal; outputting the digital pulse voltage signal to a gate terminal of a field effect transistor in order to control the field effect transistor via a first resistor; connecting a power supply to a source terminal of the field effect transistor via a first resistor and connecting a load to a drain terminal of the field effect transistor via a second resistor in order to generate and output a pulse width modulation current signal at the load.

***Response to Arguments***

4. Applicant's arguments filed 2/27/2007 have been fully considered but they are not persuasive.

Art Unit: 2816

With respect to applicant's argument that it is improper to reject such claims under 35 USC 102b since the date associated with the AAPA is indeterminate, the Examiner disagrees. A statement by an applicant during prosecution identifying the work of another as "prior art" is an admission that that work is available as prior art against the claims, regardless of whether the admitted prior art would otherwise qualify as prior art under the statutory categories of 35 U.S.C. 102. *Riverwood Int'l Corp. v. R.A. Jones & Co.*, 324 F.3d 1346, 1354, 66 USPQ2d 1331, 1337 (Fed Cir. 2003). However, even if labeled as "prior art," the work of the same inventive entity may not be considered prior art against the claims unless it falls under one of the statutory categories. *Id.*; see also *Reading & Bates Construction Co. v. Baker Energy Resources Corp.*, 748 F.2d 645, 650, 223 USPQ 1168, 1172 (Fed. Cir. 1984) ("[W]here the inventor continues to improve upon his own work product, his foundational work product should not, without a statutory basis, be treated as prior art solely because he admits knowledge of his own work. It is common sense that an inventor, regardless of an admission, has knowledge of his own work."). Consequently, the examiner must determine whether the subject matter identified as "prior art" is applicant's own work, or the work of another. In the absence of another credible explanation, examiners should treat such subject matter as the work of another. Where the specification identifies work done by another as "prior art," the subject matter so identified is treated as admitted prior art. *In re Nomiya*, 509 F.2d 566, 571, 184 USPQ 607, 611 (CCPA 1975) (holding applicant's labeling of two figures in the application drawings as "prior art" to be an admission that what was pictured was prior art relative to applicant's improvement).

With respect to applicant's argument that AAPA fails to disclose or suggest that "the triangle wave voltage signal has a plurality of rising portions and a plurality of declining portions, and the triangle wave voltage signal only comprises odd harmonics such that a percentage of high frequency harmonics of the triangle wave voltage signal is low" as recited in amended claim 1, the Examiner disagrees. Since the signal is a ramp signal it inherently has declining portions. Since the applicant used the term "comprises" the definition of comprises allows for the circuit to contain odd harmonics as well as additional items such as even harmonics. The term low is a relative term and since it is not defined in reference to reference signal can be interpreted as anything less than high frequency harmonic maximum. Therefore the limitations of the amended claim do not distinguish it over the prior art. Arguments with respect to claims 2, 7 and 8 are not persuasive for similar reasons.

With respect to applicant's argument that Haas fails to disclose the pulse width modulation current adjustment apparatus outputs a pulse width modulation current signal, the Examiner disagrees. Since Ohm's law directly relates voltage and current, it is obvious to use the current or the voltage of an output signal.

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2816

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

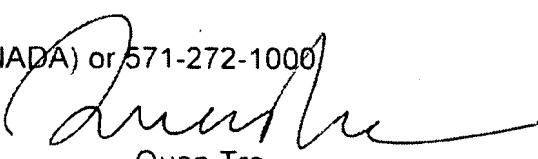
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khareem E. Almo whose telephone number is (571) 272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000

  
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Quan Tra  
PRIMARY EXAMINER

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